Docket No.: INTEL-0065 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Maged M. GHONEIMA, Peter W. CAPUTA, Muhammad M. KHELLAH, Ram KRISHNAMURTHY, James W. TSCHANZ, Yibin YE, Vivek K. DE and Yehea I. ISMAIL

Serial No.: New U.S. Patent Application

Filed: March 31, 2004 Customer No.: 34610

For: SINGLE-STAGE AND MULTI-STAGE LOW POWER INTERCONNECT ARCHITECTURES

INFORMATION DISCLOSURE STATEMENT

U.S. Patent and Trademark Office
2011 South Clark Place
Customer Window
Crystal Plaza Two, Lobby, Room 1B03
Arlington, Virginia 22202

Sir:

Pursuant to 37 C.F.R.§1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. One copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the indicated date. Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered. This statement should not be construed as a representation that a search has been made, that information cited in the statement is considered to be and/or is material to patentability, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith. It is further understood that the Examiner will consider information that was cited or submitted to the U.S. Patent and Trademark Office in a prior application relied on under 35 U.S.C. §120. 1138 OG 37, 38 (May 19, 1992).

☒ 1. This Information Disclosure Statement is being filed (i) within three months of the U.S. filing date of a U.S. application other than a CPA continued prosecution application under §1.53(d) OR (ii) within three months of the date of entry of the national stage as set forth in §1.491 in an international application OR (iii) before the mailing date of a first Office Action on the merits OR (iv) before the mailing of a first Office Action after the filing of a Request for continued examination under §1.114. No certification or fee is required. 37 C.F.R. §1.97(b).

☐ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection OR Notice of Allowance OR an action that otherwise closes prosecution in the application. 37 C.F.R. §1.97(c).

☐ a. I hereby state that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. §1.97(e)(1).

☐ b. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. §1.97(e)(2).

☐ c. Attached is our check no. _____in the amount of $180.00 in payment of the fee under 37 C.F.R. §1.17(p). Please credit or debit Deposit Account No. 16-0607 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.

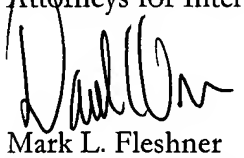
☐ 3. This Information Disclosure Statement is being filed after the mailing date of a Final Rejection OR Notice of Allowance OR an action that otherwise closes prosecution in the application, but on or before payment of the Issue Fee. Attached is our check no. _____ in the amount of $180.00 in payment of the fee under 37 C.F.R. §1.17(p). Please credit or debit Deposit Account No. 16-0607 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached. 37 C.F.R. §1.97(d).

☐ a. I hereby state that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. §1.97(e)(1).

☐ b. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. §1.97(e)(2).

☒ 4. To the extent necessary, a petition for an extension of time under 37 C.F.R. §1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

FLESHNER & KIM, LLP
Attorneys for Intel Corporation



Mark L. Fleshner
Registration No.34,596
David C. Oren
Registration No. 38,694

Correspondence Address:
P.O. Box 221200
Chantilly, VA 20153-1200
Telephone: (703) 766-3701
Date: March 31, 2004
Please direct all correspondence to Customer Number 34610

LIST OF PRIOR ART CITED BY APPLICANT

(PTO-1449)

ATTY. DOCKET NO.	APPLN. SERIAL NO.
INTEL-0065	New U.S. Patent Application
APPLICANT(S) Maged M. GHONEIMA et al	
FILING DATE March 31, 2004	GROUP To be assigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	*PATENT NO.	*ISSUE DATE	*INVENTOR NAME	CLASS	SUBCLASS	FILING DATE

U.S. PATENT APPLICATION PUBLICATIONS

	*PATENT APPLN. PUB. NO.	*PUB. DATE	*APPLICANT	CLASS	SUBCLASS	

U.S. PATENT APPLICATIONS

	*APPLN. NO.	*FILING DATE	*INVENTOR	CLASS	SUBCLASS	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Publisher, Place of Publication, Etc.)

	Rajesh Kumar et al.; "Interconnect and Noise Immunity Design for the Pentium 4 Processor;" Intel Technology Journal Q1, 2001; pp. 1-12
	Daniel Wiklund et al., "SoCBUS: Switched Network on Chip for Hard Real Time Embedded Systems;" Eight Unnumbered Pages, Date No Earlier Than 2002
	Ismail et al., "Repeater Insertion in *RLC* Lines for Minimum Propagation Delay," 1999 IEEE, pp. VI-404-VI-407
	Maged Ghoneima et al., "Utilizing the Effect of Relative Delay on Energy Dissipation in Low-Power On-Chip Buses;" pp. 1-25
	Muhammad Khellah et al., "Static Pulsed Bus for On-Chip Interconnects," 2002 Symposium on VLSI Circuits Digest of Technical Papers, pp. 78-79, 2002
	Youngsoo Shin et al, "Coupling-Driven Bus Design for Low-Power Application-Specific Systems" DAC2001, June 18-22, 2001, Las Vegas, Nevada
	Mircea R. Stan, et al, "Bus-Invert Coding for Low-Power I/O," IEEE Transactions on Very Large Scale Integration (VLSI) systems, Vol. 3, No. 1, March 1995
	Kei Hirose et al., "A Bus Delay Reduction Technique Considering Crosstalk," 5 unnumbered pages, Date No Earlier Than 1999

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.